

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 851-0001
US Patent & Trademark Office, U.S. DEPARTMENT OF COMMERCE

Complete if Known

Application Number	Unknown 10/621,253
Filing Date	Even Date Herewith
First Named Inventor	Kale, Sudhakar
Group Art Unit	Unknown 2825
Examiner Name	Unknown TUYEN TO

Sheet 1 of 2

Attorney Docket No: 884.142US2

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
TT	US-5,652,874	07/29/1997	Upson, et al.	395	500	06/07/1995
TT	US-5,737,237	04/07/1998	Tanaka, et al.	364	491	02/16/1996
TT	US-5,838,583	11/17/1998	Varadarajan, Ravi, et al.	364	491	04/12/1996
TT	US-5,898,595	04/27/1999	Bair, et al.	364	491	05/26/1995
TT	US-5,910,898	06/08/1999	Johannsen,	364	489	12/14/1995
TT	US-5,926,398	07/20/1999	Nakamura, Takeshi	364	491	03/03/1997
TT	US-5,930,499	07/27/1999	Chen, Yulin, et al.	395	500.09	05/20/1996
TT	US-5,991,524	11/23/1999	Belkhale, et al.	395	500.19	04/14/1997
TT	US-6,066,178	05/23/2000	Bair, O. S., et al.	716	2	04/10/1996
TT	US-6,148,433	11/14/2000	Chowdhary, A., et al.	716	1	11/06/1998
TT	US-6,189,131	02/13/2001	Graef, S., et al.	716	8	01/14/1998
TT	US-6,230,303	05/08/2001	Dave, B. P.	716	7	02/17/1998
TT	US-6,237,129	05/01/2001	Patterson, et al.	716	8	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
--------------------	---------------------	------------------	---	-------	----------	----------------

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume+issue number(s), publisher, city and/or country where published.	T ⁴
TT		ARIKATI, SRINIVASA R., et al., "A Signature Based Approach to Regularity Extraction", Proceedings IEEE International Conference on CAD, (Nov. 1997), 542-545	
TT		CHOWDHARY, AMIT, et al., "A General Approach for Regularity Extraction in Datapath Circuits", ICCAD, (Nov. 1998),	
TT		CHOWDHARY, AMIT, et al., "Extraction of Functional Regularity in Datapath Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 18, (Sept. 1999), 1279-1296	
TT		CHOWDHARY, AMIT, et al., "Extraction of Functional Regularity in Datapath Circuits", IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 18, NO. 9, SEPTEMBER 1999, XP-002191876, 1279-1296	
TT		CHOWDHARY, AMIT, et al., "Technology Mapping for Field-Programmable Gate Arrays Using Integer Programming", Proceedings IEEE International Conference on CAD, (Nov. 1995), 346-352	
TT		CORAZAO, MIGUEL R., et al., "Performance Optimization Using Template Mapping for Datapath-Intensive High-Level Synthesis", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, 8, (Aug.	

EXAMINER

Tuyen To

DATE CONSIDERED

07/09/2006

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

BEST AVAILABLE COPY

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**
 (Use as many sheets as necessary)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

PTO/SB/084/10-01
 Approved for use through 10/31/2002, OMB 051-0001
 US Patent & Trademark Office, U.S. DEPARTMENT OF COMMERCE

Complete if Known Application Number Filing Date First Named Inventor Group Art Unit Examiner Name	Unknown- 10/621,253
	Even Date Herewith
	Kale, Sudhakar
	Unknown 2825
	Unknown TUYEN TO
Sheet 2 of 2	Attorney Docket No: 884.142US2

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
		1996), 877-888	
TT		DETJENS, EWALD, et al., "Technology Mapping in MIS", <u>Proceedings IEEE International Conference on CAD</u> , (1987), 116-119	
TT		DOBBERPUHL, DANIEL W., "Circuits and Technology for Digital's StrongARM and ALPHA Microprocessors", <u>Proceedings Seventeenth Conference on Advanced Research in VLSI</u> , (Sept. 15-16 1997), 2-11	
TT		GUPTA, RAJESH K., et al., "Using a Programming Language for Digital System Design", <u>IEEE Design & Test of Computers</u> , (April 1997), 72-80	
TT		HANSEN, MARK C., et al., "High-Level Test Generation using Physically-Induced Faults", <u>13th IEEE VLSI Test Symposium</u> , (May 1995), 20-28	
TT		HIRSCH, MARK, et al., "Automatically Extracting Structure from a Logical Design", <u>Proceedings IEEE International Conference on CAD</u> , (Nov. 1988), 456-459	
TT		KEUTZER, KURT, "DAGON: Technology Binding and Local Optimization by DAG Matching", <u>Proceedings 24th Design Automation Conference</u> , (June 1987), 341-347	
TT		LI, JIAN, et al., "HDL Code Restructuring Using Timed Decision Tables", <u>Proceedings of the Sixth International Workshop on Hardware/Software Codesign</u> , (March 1998), 131-135	
TT		NIJSSEN, R.X.T., et al., "GreyHound: A Methodology for Utilizing Datapath Regularity in Standard Design Flows", <u>INTEGRATION, the VLSI Journal</u> 25, (1998), 111-135	
TT		NIJSSEN, R.X.T., et al., "Regular Layout Generation of Logically Optimized Datapaths", <u>Proceedings International Symposium on Physical Design</u> , (1997), 42-47	
TT		ODAWARA, GOTARO, et al., "Partitioning and Placement Technique for CMOS Gate Arrays", <u>IEEE Transactions on Computer-Aided Design</u> , Vol. CAD-6, 3, (May 1987), 355-363	
TT		RABAEY, J. M., et al., "Fast Prototyping of Datapath-Intensive Architectures", <u>IEEE Design & Test of Computers</u> , (June 1991), 40-51	
TT		RAO, D. SREENIVASA, et al., "An Approach to Scheduling and Allocation Using Regularity Extraction", <u>IEEE</u> , (1993), 557-531	
TT		RAO, D. S., et al., "On Clustering for Maximal Regularity Extraction", <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , Vol. 12, 8, (Aug. 1993), 1198-1208	
TT		YALCIN, HAKAN, et al., "An Approximate Timing Analysis Method for Datapath Circuits", <u>Proceedings IEEE International Conference on CAD</u> , (Nov. 1996), 114-118	

EXAMINER

Tuyen To

DATE CONSIDERED

07/09/2006

Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional). Applicant is to place a check mark here if English language Translation is attached.

BEST AVAILABLE COPY